PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2004-031526
(43)Date of publication of application : 29.01.2004

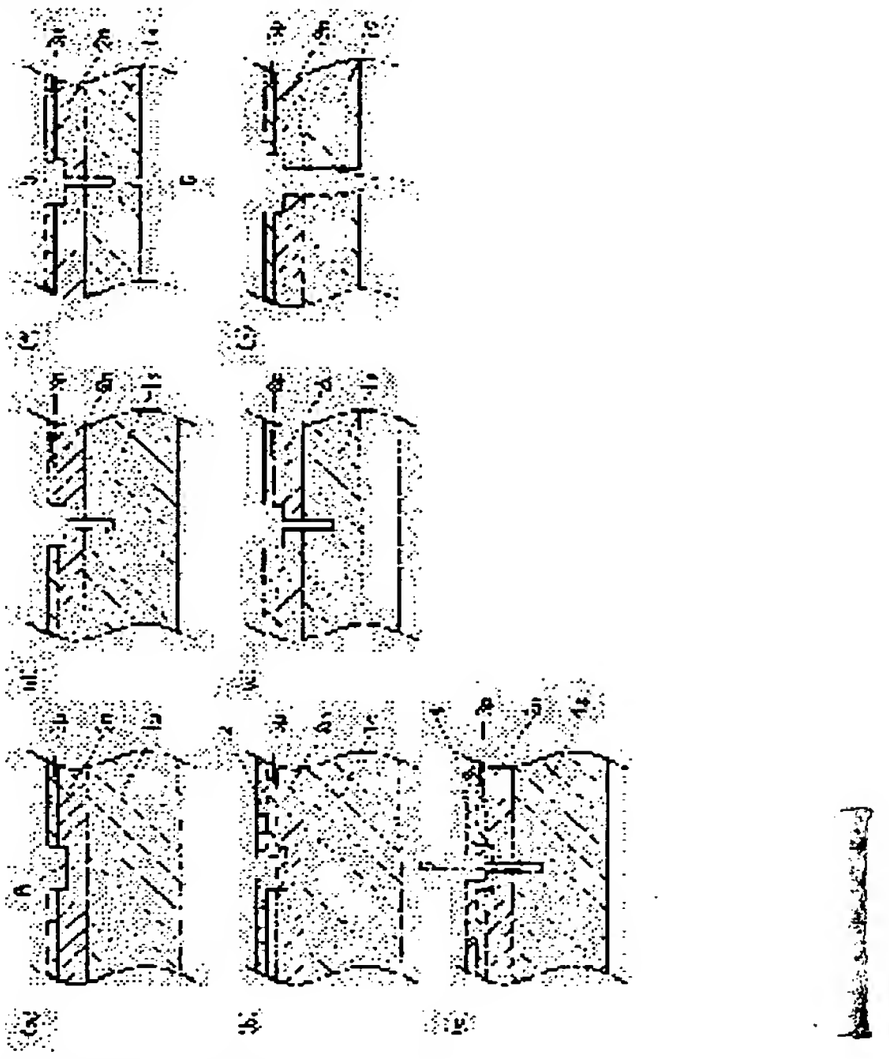
(51)Int.Cl. H01L 21/301
H01L 33/00

(21)Application number : 2002-183730
(22)Date of filing : 24.06.2002

(71)Applicant : TOYODA GOSEI CO LTD
(72)Inventor : HASHIMURA MASAKI

(54) MANUFACTURING METHOD OF GROUP III NITRIDE COMPOUND SEMICONDUCTOR ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a method of separating a group III nitride compound semiconductor element, in which there are few element cracks and fragments and which has excellent yield.
SOLUTION: The group III nitride compound semiconductor layers in a plurality of layers are formed on a substrate 1s, and elements are formed and electrodes are formed. (a) The state in which only an electrode forming layer on the side near to the substrate is left by an etching or a dicing by a dicer on an isolation line (the two group III nitride compound semiconductor layers 2n and 3p are represented.) or the state in which there is no III nitride compound semicoductor layer on the isolation line are formed. (b) A protective film 4 is formed on the whole surface, and (c) an isolation groove 5 is formed to the substrate 1s by a laser. (d) The protective film 4 is removed together with a reactant by the laser, and (e) the rear of the substrate 1s is polished and the substrate 1s is thinned. (f) A rear groove 6 is formed so as to correspond to the lattice frame-shaped isolation line of the rear of the substrate 1s, and (g) separate element is isolated along the isolation line.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]
[Claim 1]
In the manufacture approach which separates 3 group nitride system compound semiconductor element formed on the substrate, and is used as each 3 group nitride system compound semiconductor element,
The semi-conductor layer removal process made into the condition that only the electrode formative layer of a side with 3 group nitride system compound semiconductor layer near said substrate on a separation line was left behind, or the condition that there is no 3 group nitride system compound semiconductor layer on a separation line,
The protective coat formation process which forms a wrap and a protective coat removable at a next process for a substrate front-face side layer,
The laser scan process which scans a laser beam along with a separation line, and forms a separation slot,
It has removal processes, such as a protective coat which removes the discard produced by said protective coat and laser-beam scan,
The manufacture approach of 3 group nitride system compound semiconductor element characterized by separating a substrate for every component using the separation slot formed of the scan of a laser beam along with the separation line, and considering as each 3 group nitride system compound semiconductor element.
[Claim 2]
Said semi-conductor layer removal process is the manufacture approach of 3 group nitride system compound semiconductor element according to claim 1 characterized by being carried out according to the electrode formation etching process at which the electrode formation section of the electrode formative layer of the side near said substrate is exposed by etching.
[Claim 3]
Said semi-conductor layer removal process is the manufacture approach of 3 group nitride system compound semiconductor element according to claim 1 characterized by removing by dicing to the part by the side of the electrode formative layer of said substrate on a separation line.
[Claim 4]
The manufacture approach of 3 group nitride system compound semiconductor element given in any 1 term of claim 1 characterized by forming a rear-face slot in a substrate rear face so that it may correspond to said separation slot after removal processes, such as said protective coat, thru/or claim 3.
[Claim 5]
The manufacture approach of 3 group nitride system compound semiconductor element given in any 1 term of claim 1 characterized by carrying out the thinning of the substrate by polish from a rear face after removal processes, such as said protective coat, and only for the separation slot formed in the substrate front face separating a substrate for every component, and considering as each 3 group nitride system compound semiconductor element thru/or claim 3.
[Claim 6]
The manufacture approach of 3 group nitride system compound semiconductor element given in any 1 term of claim 1 characterized by forming a rear-face slot in a substrate rear face so that it may correspond to said separation slot after carrying out the thinning of the substrate by polish from a rear face after removal processes, such as said protective coat, thru/or claim 3.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]
This invention relates to the manufacture approach of 3 group nitride system compound semiconductor element formed on the substrate. Especially this invention separates 3 group nitride system compound semiconductor formed on the substrate with an easily and sufficient step stop, and relates to the production process for obtaining each 3 group nitride system compound semiconductor element.
[0002]
[Description of the Prior Art]
In manufacture of 3 group nitride system compound semiconductor element, for example, manufacture of blue LED etc., sapphire, a spinel, etc. are used as a substrate. In case these divide a wafer in order to divide into each component 3 group nitride system compound semiconductor wafer formed on the substrate since processing was not easy unlike silicon or a gallium arsenide, unlike other semiconductor devices, difficulty is accompanied by them.
[0003]
For example, the separation slot which reaches a depth of about 10 micrometers from a removal or substrate front-face side in a part of 3 group nitride system compound semiconductor layer on a separation line was formed by the dicer [side / component forming face] using a diamond blade (the so-called half cutting), and it was carrying out forming and carrying out roller breaking of the shallow rear-face slot to a rear face with a scriber etc. Under the present circumstances, after grinding the rear face and making a wafer with a thickness of 300 micrometers into about 100 micrometers in thickness after component formation, the rear-face slot was formed in many cases. Consequently, there were many what carried out the method of a crack which does not function as a component on the occasion of separation (component crack), and things which what a part of periphery is missing and it is hard to accept to be a normal article (KAKE) produces about 5%. When setting to 10 micrometers the separation depth of flute which reaches the substrate by the dicer, 20-30 micrometers is required for the width of face. Although the fault resulting from the method of a crack of a substrate will be reduced on the other hand if the depth from a substrate front face is enlarged, width of face also must be expanded to make it still deeper. Saying that width of face required for separation is enlarged means reducing the number of the semiconductor device obtained from one wafer. Furthermore, although the time amount and conditioning of rear-face polish must be changed as opposed to the wafer of different thickness, it is a very complicated activity accompanied by trial-and-error. By the way, although the various proposals (patent No. 3230572 etc.) of what forms a separation slot by the laser beam are made, it has not resulted in utilization in manufacture of 3 group nitride system compound semiconductor element.
[0004]
[Problem(s) to be Solved by the Invention]
Only in only forming a separation slot by the laser beam, slot formation of laser is melting, evaporation, and a chemical reaction, and a reactant pollutes a component side as discard. Moreover, the short circuit path which is not desirable is formed, a component property will be spoiled remarkably or the fused semi-conductor will become the separation approach with very few accepted products depending on the case.
[0005]
This invention is completed based on the above-mentioned examination result, a substrate is separated with an easily and sufficient step stop, and it aims at obtaining each 3 group nitride system compound semiconductor element.
[0006]
[Means for Solving the Problem]
In the manufacture approach which according to the means according to claim 1 separates 3 group nitride system compound semiconductor formed on the substrate, and is used as each 3 group nitride system compound semiconductor element in order to solve the above-mentioned technical problem The semi-conductor layer removal process made into the condition that only the electrode formative layer of a side with 3 group nitride system compound semiconductor layer near a substrate on a separation line was left behind, or the condition that there is no 3 group nitride system compound semiconductor layer on a separation line, The protective coat formation process which forms a wrap and a protective coat removable at a next process for a substrate front-face side layer, The laser scan process which scans a laser beam along with a separation line, and forms a separation slot, It is characterized by having removal processes, such as a protective coat which removes the discard produced by the protective coat and laser-beam scan, separating a substrate for every component using the separation slot formed of the scan of a laser beam along with the separation line, and considering as each 3 group nitride system compound semiconductor element. A separation line means the grid frame-like line at the time of seeing the separation side (however, perpendicular to a substrate or a wafer side) of the ideal for separating all 3 group nitride system compound semiconductor elements separately from a wafer from a substrate, wafer front-face, or rear-face side here.
[0007]
Moreover, a means according to claim 2 is characterized by performing a semi-conductor layer removal process according to the electrode formation etching process at which the electrode formation section of the electrode formative layer of the

side near a substrate is exposed by etching. Moreover, a means according to claim 3 is characterized by a semi-conductor layer removal process removing even the part by the side of the electrode formative layer of the substrate on a separation line by dicing.
[0008]
Moreover, a means according to claim 4 is characterized by forming a rear-face slot in a substrate rear face so that it may correspond to a separation slot after removal processes, such as a protective coat. Moreover, a means according to claim 5 is characterized by carrying out the thinning of the substrate by polish from a rear face after removal processes, such as a protective coat, and only for the separation slot formed in the substrate front face separating a substrate for every component, and considering as each 3 group nitride system compound semiconductor element. Moreover, after it carried out these with combination and it carries out the thinning of the substrate by polish from a rear face, a means according to claim 6 is characterized by forming a rear-face slot in a substrate rear face so that it may correspond to the already formed separation slot.
[0009]
[Function and Effect(s) of the Invention]
It can prevent that the melt by the laser scan of 3 group nitride system compound semiconductor layer and a reactant produce a short circuit between the layers which should contact a respectively different electrode by considering as the condition that only the electrode formative layer of a side with 3 group nitride system compound semiconductor layer near a substrate on a separation line was left behind, or the condition that there is no 3 group nitride system compound semiconductor layer on a separation line. Moreover, it can prevent that the melt of the substrate produced by laser scan or 3 group nitride system compound semiconductor layer and a reactant adhere to a semiconductor device by forming a protective coat. It can prevent producing a short circuit between the layers which should contact a polar electrode which is respectively different especially. Thus, without producing fault in the electrical property of 3 group nitride system compound semiconductor element etc., width of face is fixed, is thin, and can form a deep separation slot. That is, adjustment of the separation depth of flute is enabled by the scan speed or the count of multiplex, and the separation slot of the depth according to a deep separation slot and the thickness of a wafer with fixed width of face, or the curvature of a wafer can be formed easily. Moreover, on the occasion of formation of the deep separation slot concerned, exfoliation of 3 group nitride system compound semiconductor layer and a substrate does not arise. The blades and pure water which are an article of consumption required for formation of the separation slot of the same depth can be reduced, and a manufacturing cost can be held down. Laser with a beam diameter of 20 micrometers or less is available, and it can do more narrowly than the width of face of the separation slot produced in dicing in the case of formation of the separation slot of the same depth, for example, spacing of a luminescence side can already be set to 60 micrometers or less in a light emitting device now (claim 1).
[0010]
Before forming a separation slot, if other electrode layers on a separation line are removed, it is not necessary to establish independently the semi-conductor layer removal process for preventing the short circuit between different layers by laser scan, and a routing can be shortened according to the electrode formation etching process at which the electrode formation section of the electrode formative layer of the side near a substrate is exposed by etching (claim 2). Moreover, if dicing removes even the part by the side of the electrode formative layer of a substrate at least, it is possible to delete a substrate surface in the desired depth by conditioning (claim 3).
[0011]
Along with a separation line, a separation side can be certainly formed in a substrate rear face by forming a rear-face slot so that it may correspond to a separation slot (claim 4). Moreover, if the thinning of the substrate is carried out by polish from a rear face, it is also possible only for the separation slot formed in the substrate front face to separate a substrate for every component easily, and to consider as each 3 group nitride system compound semiconductor element (claim 5). If a rear-face slot is formed in a substrate rear face so that it may correspond to the already formed separation slot after carrying out the thinning of the substrate by polish from a rear face combining these, a substrate can be more certainly separated for every component, it can consider as each 3 group nitride system compound semiconductor element, and formation of the front-face side separation slot by laser scan can also make a laser scan quick shallowly (claim 6).
[0012]
[Embodiment of the Invention]
Hereafter, the gestalt of desirable operation of this invention is explained, referring to a drawing. In addition, this invention is not limited to the operation gestalt and example which are explained below. Moreover, in drawing 1 thru/or drawing 3 , based on drawing 1 thru/or drawing 3 , this invention is applicable [in order to explain the essence of this invention drawing simplified extremely is used but] to the manufacture approach of the usual 3 group nitride system compound semiconductor element as explained below.
[0013]
[The gestalt of the 1st operation]
Drawing 1 is process drawing (sectional view) for explaining the gestalt of operation of the 1st of this invention. Two or more layers 3 group nitride system compound semiconductor layer is formed in 1s of substrates, and a component configuration and electrode formation are performed to them. Although it is made to represent with two 3 group nitride system compound semiconductor layers 2n and 3p, by drawing 1 , this means the layer which must not be short-circuited, and does not mean only two-layer 3 group nitride system compound semiconductor layer by it. Next, the condition that only the electrode formative layer of the side near a substrate was left behind by the dicing by etching or the dicer etc. on the separation line is made ((a) of drawing 1). That is, Crevice A is formed. A separation line means the grid frame-like line at the time of seeing the separation side (however, perpendicular to substrate 1s page) of the ideal for separating all 3 group nitride system compound semiconductor elements separately from 1s of substrates from a 1s front-face [of substrates], or rear-face side here. Although considered as the condition of leaving only 2n only of electrode formative layers of the side near a substrate, in (a) of drawing 1 , of course, the dicing by etching or the dicer etc. may be performed until 1s of substrates is exposed, or until it removes 1s of some substrates. Next, in order to prevent adhesion of the reactant of 1s of

substrates by laser etc., a protective coat 4 is formed in all front faces ((b) of drawing 1). In the case of formation of the separation slot 5 by laser scan, if a protective coat 4 cannot be easily fused in the part equivalent to which laser is not, and can be removed at a next process and it does not have a bad influence on the property of a semiconductor device, its thing of arbitration is usable.

[0014]

Next, the separation slot 5 is formed in 1s of substrates with laser ((c) of drawing 1). The separation slot 5 is formed in the front-face side (side in which the component was formed) of 1s of substrates, in the shape of a grid frame along with a grid frame-like separation line. The separation slot 5 is good to consider as the 1/5 or more-about depth of the thickness after carrying out the thinning of the 1s of the substrates by polish at a next process. In addition, what is necessary is to combine the thickness of 1s of substrates removed by that cause, and the depth deleted by laser scan, and just to consider as the 1/5 or more-about depth of the thickness after carrying out the thinning of the 1s of the substrates by polish at a next process, when performing the dicing by etching or the dicer etc. until it removes 1s of some substrates. . Next, a protective coat 4 is removed with the reactant by laser ((d) of drawing 1).

[0015]

Next, 1s rear face of substrates is ground, and the thinning of the 1s of the substrates is carried out ((e) of drawing 1). Next, the rear-face slot 6 is formed in the location corresponding to the separation line of the shape of a grid frame of the rear face of 1s of substrates ((f) of drawing 1). What is necessary is just to form a shallow slot with a scriber etc. about the formation approach of the rear-face slot 6 unlike ******** 5. After [this] roller breaking etc. separates into each component along with a grid frame-like separation line. In this case, since the depth of the separation slot 5 is about [of 1s of substrates which carried out thinning / 1/5 or more], the separation side 7 becomes what connected the separation slot 5 which certainly met the grid frame-like separation line, and the rear-face slot 6. That is, being divided in the direction which is not desirable as for the direction of slant etc. is prevented ((g) of drawing 1).

[0016]

[The gestalt of the 2nd operation]

Drawing 2 is process drawing (sectional view) for explaining the gestalt of operation of the 2nd of this invention. The condition that only the electrode formative layer of the side near a substrate was left behind by the dicing by etching or the dicer etc. on the separation line like the gestalt of operation of the 1st of drawing 1 is made ((a) of drawing 2). In this case, of course [until 1s of substrates is exposed, or until it removes 1s of some substrates], the dicing by etching or the dicer etc. may be performed. Next, the protective coat 4 removable at a next process is formed in all front faces ((b) of drawing 2). Next, with this operation gestalt, the 5d of the 1st slot of the 1/5 or more-about depth of the thickness of 1s of substrates is formed in the front-face side (side in which the component was formed) of 1s of substrates, in the shape of a grid frame along with a grid frame-like separation line ((c) of drawing 2). Next, a protective coat 4 is removed with the reactant by laser ((d) of drawing 2).

[0017]

Next, the rear-face slot 6 is formed so that it may correspond to the separation line of the shape of a grid frame of the rear face of 1s of substrates ((e) of drawing 2). The formation approach of the rear-face slot 6 should just form a shallow slot with a scriber etc. like the thing in the gestalt of the 1st operation. After [this] roller breaking etc. separates into each component along with a grid frame-like separation line. Since it is about [that the depth of 5d of separation slots is 1s of substrates / 1/5 or more], the separation side 7 becomes what connected 5d of separation slots which certainly met the grid frame-like separation line, and the rear-face slot 6 ((f) of drawing 2).

[0018]

[The gestalt of the 3rd operation]

Drawing 3 is process drawing (sectional view) for explaining the gestalt of operation of the 3rd of this invention. The condition that only the electrode formative layer of the side near a substrate was left behind by the dicing by etching or the dicer etc. on the separation line like the gestalt of operation of the 2nd of drawing 2 is made ((a) of drawing 3). In this case, of course [until 1s of substrates is exposed, or until it removes 1s of some substrates], the dicing by etching or the dicer etc. may be performed. Next, the protective coat 4 removable at a next process is formed in all front faces ((b) of drawing 3). Next, the 5d of the 1st slot of the depth more than thickness extent after carrying out the thinning of the 1s of the substrates by polish at a next process is formed in the front-face side (side in which the component was formed) of 1s of substrates, in the shape of a grid frame along with a grid frame-like separation line ((c) of drawing 3). Next, a protective coat 4 is removed with the reactant by laser ((d) of drawing 3).

[0019]

Next, the pressure sensitive adhesive sheet 8 of one sheet is stuck on the whole 1s front face of substrates, is turned over, 1s rear face of substrates is ground, and the thinning of the 1s of the substrates is carried out ((e) of drawing 3). If the thinning of the 1s of the substrates is carried out and thinning is carried out to below the depth of the separation slot 5, each component is separable with the separation slot 5 which certainly met the grid frame-like separation line ((f) of drawing 3).

[0020] [The 1st example]

Drawing 4 is process drawing (sectional view) for explaining the 1st concrete example of this invention in which the yield and component property of a crack and KAKE are evaluated and which went to accumulate. On silicon on sapphire 1 with a thickness of about 300 micrometers, the laminating of the 3 group nitride system compound semiconductor layer was carried out, and about 3000 blue LED components of pn double heterojunction were formed. It simplifies about the laminated structure of the component part concerned, and the sign 2 of 1 shows. there is no electrode **** -- coming out, the total thickness of 3 group nitride system compound semiconductor layer is about 5 micrometers. First, the inside of each grid formed 10 micrometers of deepest parts, and the 1st slot A of 30 micrometers of **** by the dicer which uses a diamond blade along with the separation line of the shape of a grid frame used as the blue LED component of one. At this time, about 5 micrometers of silicon on sapphire 1 were deleted in the deepest part B of the 1st slot A.

[0021]

Next, transparence resin 4 was applied all over the component forming face, and was stiffened. Next, using the 3rd higher

harmonic wave (wavelength of 355nm) of an YAG laser, the laser beam with a beam diameter of about 20 micrometers was irradiated along with the separation line, and the 2nd slot C deeper 10 more micrometers than the 1st slot A was formed. In this way, the separation slot 5 which deleted about 15 micrometers of silicon on sapphire 1 by the 1st slot A and the 2nd slot C was formed. Then, the rear face of silicon on sapphire 1 was ground, and the thinning of the silicon on sapphire 1 was carried out to 100 micrometers. Next, the separation slot 6 was formed in the rear face of silicon on sapphire 1 with the scriber. Then, silicon on sapphire was broken by roller breaking, and it separated into each blue LED component. Under the present circumstances, the defect-of-shape article (the so-called component crack, KAKE) by breaking silicon on sapphire 1 itself is ten or less pieces, and each light emitting device did not have a difference in the blue LED component and component property which were separated without using laser.

[0022]

[The example 1 of a comparison]

When a front face was made into scribing after grinding dicing and a rear face and also isolation was performed like the 1st example of the above without using laser, 100 or more defect-of-shape articles (the so-called component crack, KAKE) were produced.

[0023]

[The example 2 of a comparison]

When dicing should be performed for the separation slot on surface only using laser and also isolation was performed like the 1st example of the above, there were few defectives (the so-called component crack, KAKE), and they were good. However, since the short circuit of p electrode side layer and n electrode side layer arose, also when it was any, the defect of a component property arose in large quantities. Moreover, the fundamental wave (1064nm) of an YAG laser, and in the case of about 15-micrometer beam diameter, the same result was obtained.

[Brief Description of the Drawings]

[Drawing 1] Process drawing for explaining the gestalt of operation of the 1st of this invention (sectional view).

[Drawing 2] Process drawing for explaining the gestalt of operation of the 2nd of this invention (sectional view).

[Drawing 3] Process drawing for explaining the gestalt of operation of the 3rd of this invention (sectional view).

[Drawing 4] Process drawing for explaining the 1st concrete example of this invention (sectional view).

[Description of Notations]

1 1s Substrate

2 3 Group Nitride System Compound Semiconductor Layer Which Carried Out Laminating

2n The electrode formative layer near a substrate (3 group nitride system compound semiconductor layer)

3p 3 group nitride system compound semiconductor layer

4 Protective Coat

5 5d Separation slot

6 Rear-Face Slot

7 Separation Side

8 Pressure Sensitive Adhesive Sheet

A A crevice or the 1st slot

B The deepest part of the 1st slot

C The 2nd slot

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Process drawing for explaining the gestalt of operation of the 1st of this invention (sectional view).
[Drawing 2] Process drawing for explaining the gestalt of operation of the 2nd of this invention (sectional view).
[Drawing 3] Process drawing for explaining the gestalt of operation of the 3rd of this invention (sectional view).
[Drawing 4] Process drawing for explaining the 1st concrete example of this invention (sectional view).
[Description of Notations]
1 1s Substrate
2 3 Group Nitride System Compound Semiconductor Layer Which Carried Out Laminating
2n The electrode formative layer near a substrate (3 group nitride system compound semiconductor layer)
3p 3 group nitride system compound semiconductor layer
4 Protective Coat
5 5d Separation slot
6 Rear-Face Slot
7 Separation Side
8 Pressure Sensitive Adhesive Sheet
A A crevice or the 1st slot
B The deepest part of the 1st slot
C The 2nd slot

[Translation done.]

(19)日本国特許庁(JP)

(12)公開特許公報(A)

(11)特許出願公開番号
特開2004-31526
(P2004-31526A)
(43)公開日 平成16年1月29日(2004.1.29)

(51)Int.Cl.[7]	F I		テーマコード（参考）
H01L 21/301	H01L 21/78	A	5F041
H01L 33/00	H01L 33/00	C	
	H01L 21/78	B	

審査請求 未請求　請求項の数 6　OL　（全 8 頁）

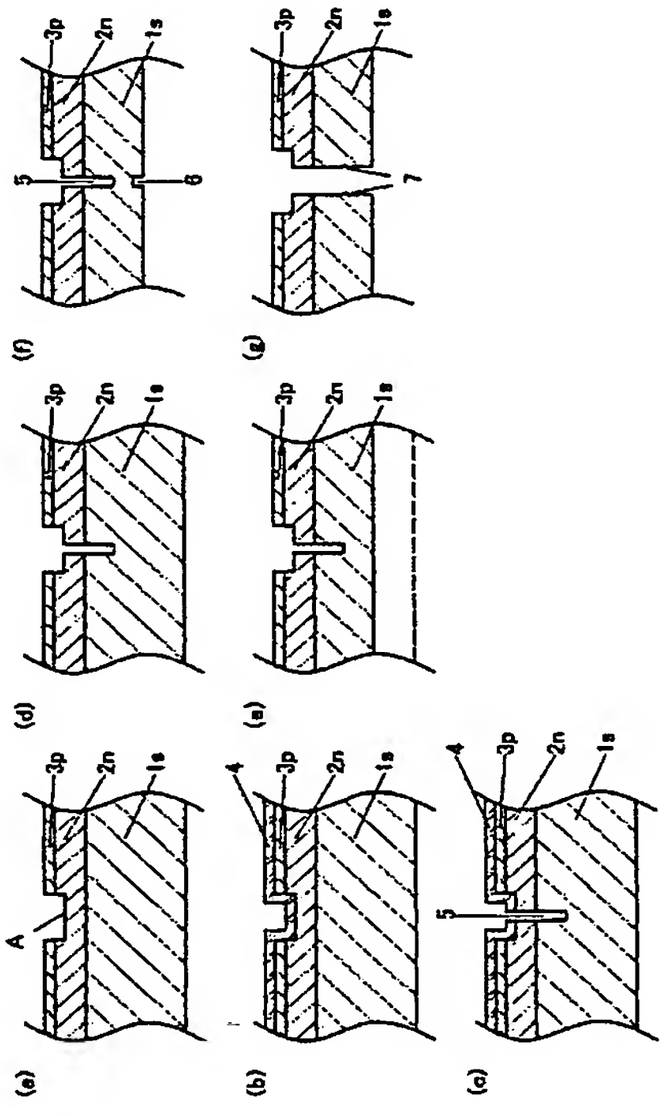
(21)出願番号　特願2002-183730(P2002-183730)
(22)出願日　平成14年6月24日(2002.6.24)

(71)出願人　000241463
豊田合成株式会社
愛知県西春日井郡春日町大字落合字長畑1番地
(74)代理人　100087723
弁理士　藤谷　修
(72)発明者　橘村　昌樹
愛知県西春日井郡春日町大字落合字長畑1番地　豊田合成株式会社内

Fターム(参考)　5F041 CA40 CA74 CA75 CA76 CA77

(54)【発明の名称】３族窒化物系化合物半導体素子の製造方法

(57)【要約】
【課題】素子ワレ、カケの少ない、歩留まりの良い３族窒化物系化合物半導体素子の分離方法を提供する。
【解決手段】基板１ｓに、複数層の３族窒化物系化合物半導体層を形成し、素子形状及び電極形成を行う。（２つの３族窒化物系化合物半導体層２ｎと３ｐで代表させている。）分離線上に、エッチング又はダイサーによるダイシング等で、基板に近い側の電極形成層のみ残された状態、又は分離線上の３族窒化物系化合物半導体層が無い状態を作る（ａ）。保護膜４を全表面に形成し（ｂ）、レーザーにより、基板１ｓに、分離溝５を形成する（ｃ）。保護膜４をレーザーによる反応物とともに除去し（ｄ）、基板１ｓ裏面を研磨し、基板１ｓを薄膜化する（ｅ）。次に基板１ｓの裏面の格子枠状の分離線に対応するように、裏面溝６を形成し（ｆ）、分離線に沿って個々の素子に分離する（ｇ）。
【選択図】　図１



【特許請求の範囲】
【請求項１】
基板上に形成された３族窒化物系化合物半導体素子を分離して個々の３族窒化物系化合物半導体素子とする製造方法において、
分離線上の３族窒化物系化合物半導体層が前記基板に近い側の電極形成層のみ残された状態、又は分離線上の３族窒化物系化合物半導体層が無い状態とする半導体層除去工程と、
基板表面側層を覆う、後の工程で除去可能な保護膜を形成する保護膜形成工程と、
分離線に沿ってレーザービームを走査して分離溝を形成するレーザー走査工程と、
前記保護膜及びレーザービーム走査により生じた不要物を除去する保護膜等除去工程とを有し、
分離線に沿ってレーザービームの走査により形成された分離溝を用いて基板を素子ごとに分離して個々の３族窒化物系化合物半導体素子とすることを特徴とする３族窒化物系化合物半導体素子の製造方法。
【請求項２】
前記半導体層除去工程は、エッチングにより前記基板に近い側の電極形成層の電極形成部を露出させる電極形成エッチング工程により行われることを特徴とする請求項１に記載の３族窒化物系化合物半導体素子の製造方法。
【請求項３】
前記半導体層除去工程は、ダイシングにより分離線上の、前記基板の電極形成層側の一部まで除去することを特徴とする請求項１に記載の３族窒化物系化合物半導体素子の製造方法。
【請求項４】
前記保護膜等除去工程以降に、前記分離溝に対応するように、基板裏面に裏面溝を形成することを特徴とする請求項１乃至請求項３のいずれか１項に記載の３族窒化物系化合物半導体素子の製造方法。
【請求項５】
前記保護膜等除去工程以降に、基板を裏面から研磨により薄肉化して、基板表面に形成された分離溝のみにより基板を素子ごとに分離して個々の３族窒化物系化合物半導体素子とすることを特徴とする請求項１乃至請求項３のいずれか１項に記載の３族窒化物系化合物半導体素子の製造方法。
【請求項６】
前記保護膜等除去工程以降に、基板を裏面から研磨により薄肉化した後、前記分離溝に対応するよう、基板裏面に裏面溝を形成することを特徴とする請求項１乃至請求項３のいずれか１項に記載の３族窒化物系化合物半導体素子の製造方法。

【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は基板上に形成された３族窒化物系化合物半導体素子の製造方法に関する。本発明は特に、基板上に形成された３族窒化物系化合物半導体を容易且つ歩止まり良く分離して、個々の３族窒化物系化合物半導体素子を得るための製造工程に関する。
【０００２】
【従来の技術】
３族窒化物系化合物半導体素子の製造、例えば青色ＬＥＤ等の製造においては、基板としてサファイアやスピネルなどが用いられている。これらはシリコンやガリウムヒ素と異なり、加工が容易でないため、基板上に形成した３族窒化物系化合物半導体ウエハを個々の素子に分離するためウエハを分割する際、他の半導体素子とは異なり困難が伴う。
【０００３】
例えば、素子形成面側をダイヤモンドブレードを用いたダイサーにより、分離線上の３族窒化物系化合物半導体層の一部を除去又は基板表面側から約１０μｍの深さに達する分離溝を形成し（いわゆるハーフカット）、裏面にスクライバーで浅い裏面溝を形成してロー

ラーブレイキングするなどしていた。この際、厚さ３００μｍのウエハを素子形成後に裏面を研磨して厚さ１００μｍ程度としてから裏面溝を形成することが多かった。その結果、分離に際し、素子として機能しないような割れ方をしたもの（素子ワレ）、周辺部が一部欠けて正常品とは認めがたいもの（カケ）が５％程度生じるものが多かった。ダイサーによる基板に達する分離溝の深さを１０μｍとする場合、その幅は２０～３０μｍが必要である。一方基板表面からの深さを大きくすると基板のワレ方に起因する不具合が低減されるが、さらに深くするには幅も広げざるを得ない。分離に必要な幅を大きくすると言うことは、１枚のウエハから得られる半導体素子の個数を減らすことを意味する。更に異なる厚さのウエハに対しては例えば裏面研磨の時間や条件設定を変えなければならないが、それは試行錯誤を伴う極めて煩雑な作業である。ところで、レーザービームにより分離溝を形成するものが各種提案（特許第３２３０５７２号等）されているが、３族窒化物系化合物半導体素子の製造において、実用化には至っていない。

【０００４】

【発明が解決しようとする課題】

単にレーザービームにより分離溝を形成するのみでは、レーザーの溝形成が溶融、蒸発、及び化学反応であって、反応物が不要物として素子面を汚染する。また、溶融した半導体が、望ましくない短絡経路を形成し、素子特性を著しく損ねたり、場合によっては合格品が極めて少ない分離方法となってしまう。

【０００５】

本発明は上記の検討結果に基づき完成されたものであって、基板を容易且つ歩止まり良く分離して、個々の３族窒化物系化合物半導体素子を得ることを目的とする。

【０００６】

【課題を解決するための手段】

上記の課題を解決するため、請求項１に記載の手段によれば、基板上に形成された３族窒化物系化合物半導体を分離して個々の３族窒化物系化合物半導体素子とする製造方法において、分離線上の３族窒化物系化合物半導体層が基板に近い側の電極形成層のみ残された状態、又は分離線上の３族窒化物系化合物半導体層が無い状態とする半導体層除去工程と、基板表面側層を覆う、後の工程で除去可能な保護膜を形成する保護膜形成工程と、分離線に沿ってレーザービームを走査して分離溝を形成するレーザー走査工程と、保護膜及びレーザービーム走査により生じた不要物を除去する保護膜等除去工程とを有し、分離線に沿ってレーザービームの走査により形成された分離溝を用いて基板を素子ごとに分離して個々の３族窒化物系化合物半導体素子とすることを特徴とする。ここで分離線とは、ウエハから全ての３族窒化物系化合物半導体素子を個々に分離するための理想の分離面（ただし基板又はウエハ面に垂直）を、基板又はウエハ表面側又は裏面側から見た場合の、格子枠状の線を意味する。

【０００７】

また、請求項２に記載の手段は、半導体層除去工程は、エッチングにより基板に近い側の電極形成層の電極形成部を露出させる電極形成エッチング工程により行われることを特徴とする。また、請求項３に記載の手段は、半導体層除去工程は、ダイシングにより分離線上の、基板の電極形成層側の一部までを除去することを特徴とする。

【０００８】

また、請求項４に記載の手段は、保護膜等除去工程以降に、分離溝に対応するように、基板裏面に裏面溝を形成することを特徴とする。また、請求項５に記載の手段は、保護膜等除去工程以降に、基板を裏面から研磨により薄肉化して、基板表面に形成された分離溝のみにより基板を素子ごとに分離して個々の３族窒化物系化合物半導体素子とすることを特徴とする。また、請求項６に記載の手段は、これらを組合せ、基板を裏面から研磨により薄肉化した後、既に形成された分離溝に対応するよう、基板裏面に裏面溝を形成することを特徴とする。

【０００９】

【作用及び発明の効果】

分離線上の３族窒化物系化合物半導体層が基板に近い側の電極形成層のみ残された状態、又は分離線上の３族窒化物系化合物半導体層が無い状態とすることで、３族窒化物系化合物半導体層のレーザー走査による溶融物、反応物が、各々異なる電極と接触すべき層の間で短絡を生じることを防止することができる。また、保護膜を形成することで、レーザー走査により生じる基板や３族窒化物系化合物半導体層の溶融物、反応物が半導体素子に付着することを防止することができる。特に、各々異なる極性の電極と接触すべき層の間で短絡を生じることを防止することができる。このようにして、３族窒化物系化合物半導体素子の電気特性等に不具合を生じることなく、幅が一定で細く、深い分離溝を形成することができる。即ち、走査速度や多重回数で分離溝の深さを調整可能とし、幅が一定な、深い分離溝やウエハの厚さやウエハの反りに応じた深さの分離溝を容易に形成することができる。また、当該深い分離溝の形成に際し３族窒化物系化合物半導体層と基板の剥離が生じない。同じ深さの分離溝の形成に必要な消耗品であるブレードや純水を削減することができ、製造コストを抑えることができる。現在既に２０μｍ以下のビーム径のレーザーが入手可能で、同じ深さの分離溝の形成の際にダイシングで生じる分離溝の幅より狭くできる、例えば発光素子においては発光面の間隔を６０μｍ以下とすることができる（請求項１）。

【００１０】

分離溝を形成する前に、エッチングにより基板に近い側の電極形成層の電極形成部を露出させる電極形成エッチング工程により、分離線上の他の電極層を除去すれば、レーザー走査による異なる層間の短絡を防ぐための半導体層除去工程を別に設ける必要がなく、作業工程が短縮できる（請求項２）。また、ダイシングにより少なくとも、基板の電極形成層側の一部までを除去すれば、条件設定により基板表層を所望の深さに削ることが可能である（請求項３）。

【００１１】

分離溝に対応するよう、基板裏面に裏面溝を形成することで、確実に分離線に沿って分離面を形成することができる（請求項４）。また、基板を裏面から研磨により薄肉化すれば、基板表面に形成された分離溝のみにより容易に基板を素子ごとに分離して個々の３族窒化物系化合物半導体素子とすることも可能である（請求項５）。これらを組合わせて、基板を裏面から研磨により薄肉化した後、既に形成された分離溝に対応するよう、基板裏面に裏面溝を形成すれば、より確実に基板を素子ごとに分離して個々の３族窒化物系化合物半導体素子とすることができ、レーザー走査による表面側分離溝の形成も、浅く且つレーザー走査を速くすることができる（請求項６）。

【００１２】

【発明の実施の形態】

以下、本発明の好ましい実施の形態について、図面を参照しつつ説明する。尚、本発明は以下に説明する実施形態、実施例に限定されるものではない。また、図１乃至図３においては、本発明の本質を説明するため、極めて簡略化した図を用いるが、以下に説明する通り、図１乃至図３に基づいて、本発明は通常の３族窒化物系化合物半導体素子の製造方法に適用できるものである。

【００１３】

〔第１の実施の形態〕

図１は、本発明の第１の実施の形態を説明するための工程図（断面図）である。基板１ｓに、複数層の３族窒化物系化合物半導体層を形成し、素子形状及び電極形成を行う。図１では、２つの３族窒化物系化合物半導体層２ｎと３ｐで代表させているが、これは短絡させてはいけない層を意味するのであって、２層の３族窒化物系化合物半導体層のみを意味するものではない。次に、分離線上に、エッチング又はダイサーによるダイシング等で、基板に近い側の電極形成層のみ残された状態を作る（図１の（ａ））。即ち、凹部Ａを形成する。ここで分離線とは、基板１ｓから全ての３族窒化物系化合物半導体素子を個々に分離するための理想の分離面（ただし基板１ｓ面に垂直）を、基板１ｓ表面側又は裏面側から見た場合の、格子枠状の線を意味する。図１の（ａ）では、基板に近い側の電極形成

層２ｎのみ残す状態としたが、基板１ｓが露出するまで、或いは基板１ｓの一部を取り除くまで、エッチング又はダイサーによるダイシング等を行って良いことはもちろんである。次に、レーザーによる基板１ｓの反応物等の付着を防止するため、保護膜４を全表面に形成する（図１の（ｂ））。保護膜４は、レーザー走査による分離溝５の形成の際、レーザーが当たらない部分では容易には溶融しないものであって、後の工程で除去可能であり、半導体素子の特性に悪影響を及ぼさないものであれば任意のものが使用可能である。

【００１４】

次に、レーザーにより、基板１ｓに、分離溝５を形成する（図１の（ｃ））。分離溝５は格子枠状の分離線に沿って基板１ｓの表面側（素子を形成した側）に格子枠状に形成される。分離溝５は、後の工程で研磨により基板１ｓを薄肉化した後の厚さの１／５程度以上の深さとすると良い。尚、基板１ｓの一部を取り除くまで、エッチング又はダイサーによるダイシング等を行う場合は、それにより取り除かれた基板１ｓの厚さとレーザー走査により削られた深さを併せて、後の工程で研磨により基板１ｓを薄肉化した後の厚さの１／５程度以上の深さとすれば良い。。次に、保護膜４をレーザーによる反応物とともに除去する（図１の（ｄ））。

【００１５】

次に、基板１ｓ裏面を研磨し、基板１ｓを薄肉化する（図１の（ｅ））。次に基板１ｓの裏面の格子枠状の分離線に対応する位置に、裏面溝６を形成する（図１の（ｆ））。裏面溝６の形成方法に関しては分離溝５と異なり、スクライバー等により浅い溝を形成すれば良い。こののちローラーブレイキング等により格子枠状の分離線に沿って個々の素子に分離する。この場合、分離溝５の深さは薄肉化した基板１ｓの１／５程度以上であるので、分離面７は確実に格子枠状の分離線に沿った、分離溝５と裏面溝６とを接続したものとなる。即ち、斜め方向などの望ましくない方向に割れることが防止される（図１の（ｇ））。

【００１６】

〔第２の実施の形態〕

図２は、本発明の第２の実施の形態を説明するための工程図（断面図）である。図１の第１の実施の形態同様、分離線上に、エッチング又はダイサーによるダイシング等で、基板に近い側の電極形成層のみ残された状態を作る（図２の（ａ））。この場合、基板１ｓが露出するまで、或いは基板１ｓの一部を取り除くまでエッチング又はダイサーによるダイシング等を行って良いことはもちろんである。次に、後の工程で除去可能な保護膜４を全表面に形成する（図２の（ｂ））。次に、本実施形態では、基板１ｓの厚さの１／５程度以上の深さの第１の溝５ｄを、格子枠状の分離線に沿って基板１ｓの表面側（素子を形成した側）に格子枠状に形成する（図２の（ｃ））。次に、保護膜４をレーザーによる反応物とともに除去する（図２の（ｄ））。

【００１７】

次に基板１ｓの裏面の格子枠状の分離線に対応するように、裏面溝６を形成する（図２の（ｅ））。裏面溝６の形成方法は第１の実施の形態におけるものと同様に、スクライバー等により浅い溝を形成すれば良い。こののちローラーブレイキング等により格子枠状の分離線に沿って個々の素子に分離する。分離溝５ｄの深さが基板１ｓの１／５程度以上であるので、分離面７は確実に格子枠状の分離線に沿った、分離溝５ｄと裏面溝６とを接続したものとなる（図２の（ｆ））。

【００１８】

〔第３の実施の形態〕

図３は、本発明の第３の実施の形態を説明するための工程図（断面図）である。図２の第２の実施の形態同様、分離線上に、エッチング又はダイサーによるダイシング等で、基板に近い側の電極形成層のみ残された状態を作る（図３の（ａ））。この場合、基板１ｓが露出するまで、或いは基板１ｓの一部を取り除くまでエッチング又はダイサーによるダイシング等を行って良いことはもちろんである。次に、後の工程で除去可能な保護膜４を全表面に形成する（図３の（ｂ））。次に、後の工程で研磨により基板１ｓを薄肉化した後

の厚さ程度以上の深さの第１の溝５ｄを、格子枠状の分離線に沿って基板１ｓの表面側（素子を形成した側）に格子枠状に形成する（図３の（ｃ））。次に、保護膜４をレーザーによる反応物とともに除去する（図３の（ｄ））。

【００１９】

次に、１枚の粘着シート８を基板１ｓ表面全体に貼り付け、裏返して基板１ｓ裏面を研磨し、基板１ｓを薄肉化する（図３の（ｅ））。基板１ｓを薄肉化して、分離溝５の深さ以下にまで薄肉化すれば、確実に格子枠状の分離線に沿った、分離溝５により個々の素子が分離できる（図３の（ｆ））。

【００２０】〔第１実施例〕

図４はワレとカケの歩留まり及び素子特性を評価するために行った、本発明の具体的な第１の実施例を説明するための工程図（断面図）である。厚さ約３００μｍのサファイア基板１上に３族窒化物系化合物半導体層を積層して、ｐｎダブルヘテロ接合の約３０００個の青色ＬＥＤ素子を形成した。当該素子部分の積層構造については簡略化し１の符号２で示す。電極含まないで、３族窒化物系化合物半導体層の総膜厚は約５μｍである。まず、ダイヤモンドブレードを使用するダイサーによって、各格子内が１の青色ＬＥＤ素子となる格子枠状の分離線に沿って、最深部１０μｍ、幅約３０μｍの第１の溝部Ａを形成した。この時、第１の溝部Ａの最深部Ｂにおいて、サファイア基板１は約５μｍ削除された。

【００２１】

次に、透明樹脂４を素子形成面の全面に塗布し、硬化させた。次にＹＡＧレーザーの第３次高調波（波長３５５ｎｍ）を用い、ビーム径約２０μｍのレーザービームを分離線に沿って照射し、第１の溝部Ａより更に１０μｍ深い第２の溝部Ｃを形成した。こうして第１の溝部Ａと第２の溝部Ｃにより、サファイア基板１を約１５μｍ削った分離溝５が形成された。この後、サファイア基板１の裏面を研磨し、サファイア基板１を１００μｍまで薄肉化させた。次にサファイア基板１の裏面にスクライバーにより分離溝６を形成した。この後、ローラーブレイキングによりサファイア基板を割り、個々の青色ＬＥＤ素子に分離した。この際、サファイア基板１を割ること自体による形状不良品（いわゆる素子ワレ、カケ）は１０個以下であり、また、各発光素子は、レーザーを用いないで分離した青色ＬＥＤ素子と素子特性に差異がなかった。

【００２２】

〔比較例１〕

レーザーを用いないで、表面をダイシング、裏面を研磨後のスクライビングとした他、上記第１実施例と同様に素子分離を行った場合、形状不良品（いわゆる素子ワレ、カケ）は１００個以上生じた。

【００２３】

〔比較例２〕

表面の分離溝をレーザーのみを用い、ダイシングを行わないものとした他、上記第１実施例と同様に素子分離を行った場合、不良品（いわゆる素子ワレ、カケ）は少なく、良好であった。しかし、ｐ電極側層とｎ電極側層の短絡が生じるため、いずれの場合も素子特性の不良が大量に生じた。又、ＹＡＧレーザーの基本波（１０６４ｎｍ）、ビーム径約１５μｍの場合においても、同様な結果が得られた。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態を説明するための工程図（断面図）。

【図２】本発明の第２の実施の形態を説明するための工程図（断面図）。

【図３】本発明の第３の実施の形態を説明するための工程図（断面図）。

【図４】本発明の具体的な第１の実施例を説明するための工程図（断面図）。

【符号の説明】

１、１ｓ　基板

２　積層した３族窒化物系化合物半導体層

２ｎ　基板に近い電極形成層（３族窒化物系化合物半導体層）

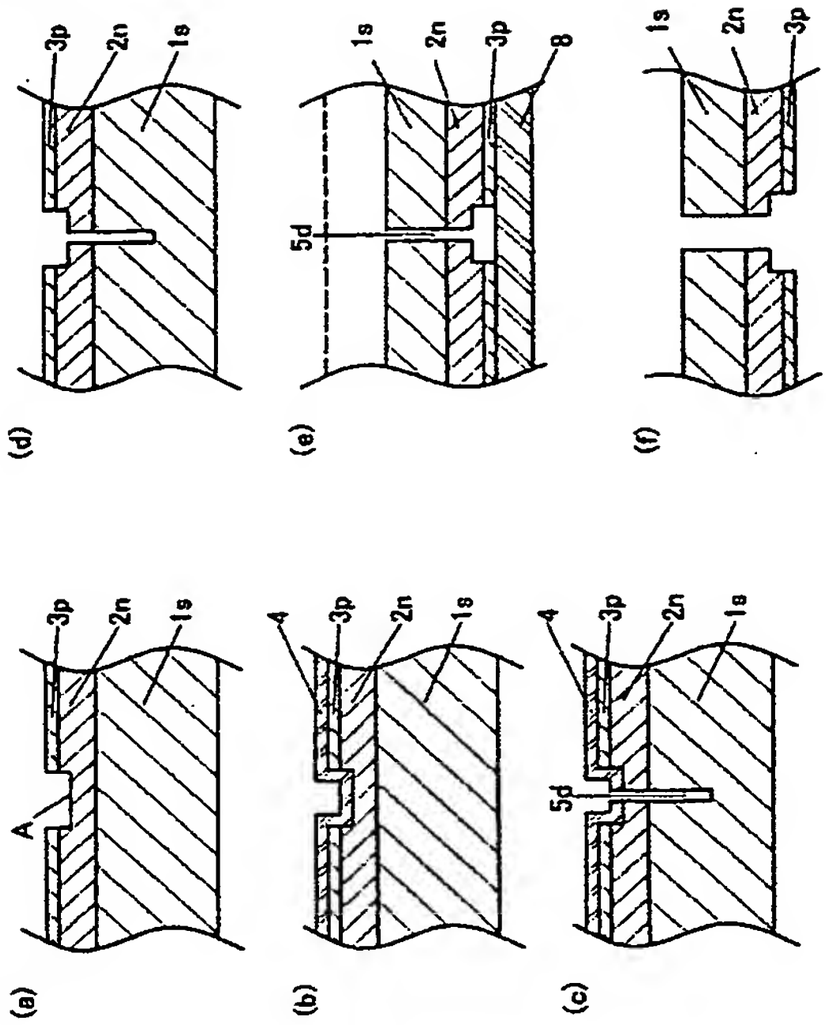
３ｐ　３族窒化物系化合物半導体層

4　保護膜
5、5d　分離溝
6　裏面溝
7　分離面
8　粘着シート
A　凹部又は第１の溝部
B　第１の溝部の最深部
C　第２の溝部

【図１】

【図２】

【図３】



【図４】